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FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 1405.1055	APPLICATION NO. 10/034,321
LIST OF REFERENCES CITED BY APPLICANT *(Use several sheets if necessary)*		FIRST NAMED INVENTOR Souichi OKADA, et al.	
		FILING DATE January 3, 2002	GROUP ART UNIT

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U.S. PATENT DOCUMENTS

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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AM	Henry Kuo, et al., "Architectural Optimization for a 1.82Gbits/see VLSI Implementation of the AES Rijndael Algorithm", Electrical Engineering Department, University of California, Los Angeles.
	AN	Máire McLoone, et al., "High Performance Single-Chip FPGA Rijndael Algorithm Implementations", DiSip™ Laboratories, School of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast BT9 5AH, Northern Ireland.

EXAMINER PRAMILA PARTHASARATHY	DATE CONSIDERED 09/14/05

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LIST OF REFERENCES CITED BY APPLICANT		FIRST NAMED INVENTOR Souichi OKADA, et al.	
(Use several sheets if necessary)		FILING DATE January 3, 2002	GROUP ART UNIT 2131

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	AK							
	AL							

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AM	M. MCLOONE et al., "High Performance Single-Chip FPGA Rijndael Algorithm Implementations", Cryptographic Hardware and Embedded Systems, 3rd International Workshop, Ches 2001, Paris, France, May 14-16, 2001, Proceedings, Lecture Notes in Computer Science, Berlin: Springer, DE, Vol. 2162, 14 May 2001 (2001-05-14), pages 65-76.
	AN	J. DAEMEN et al., "AES Proposal: Rijndael", AES Proposal, XX, SS, 3 September 1999 (1999-09-03), pages 1-45.

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